

# Low Hardware Cost Architecture of H.264/AVC Integer Motion Estimation

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## Research Theme

### Variable Block Size Motion Estimation

### Large Frame Size Video Sequence

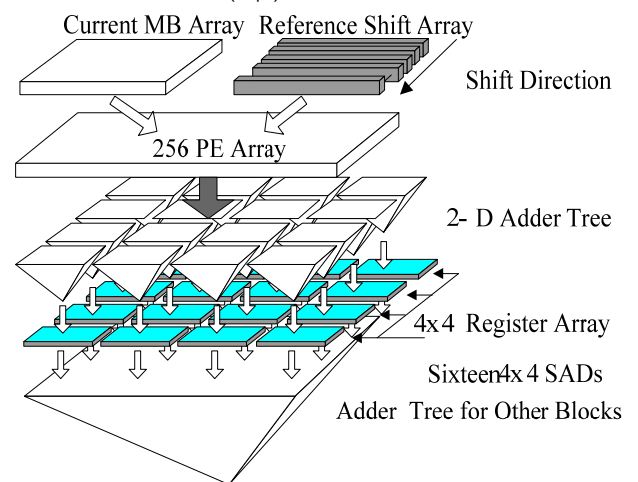
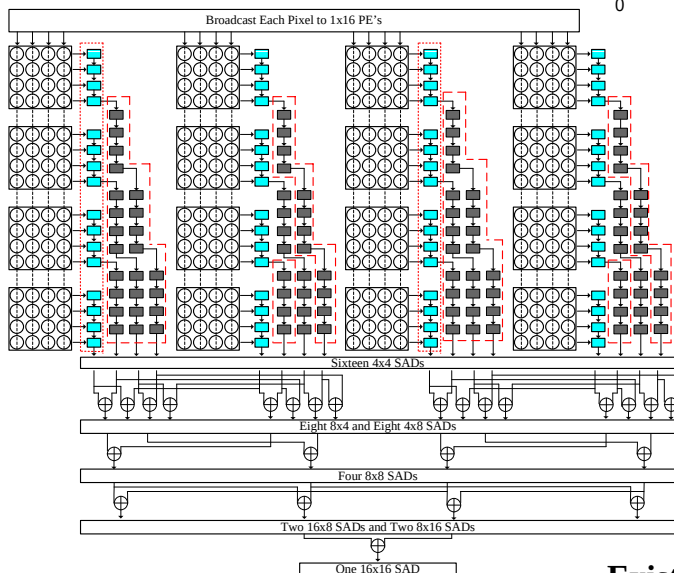
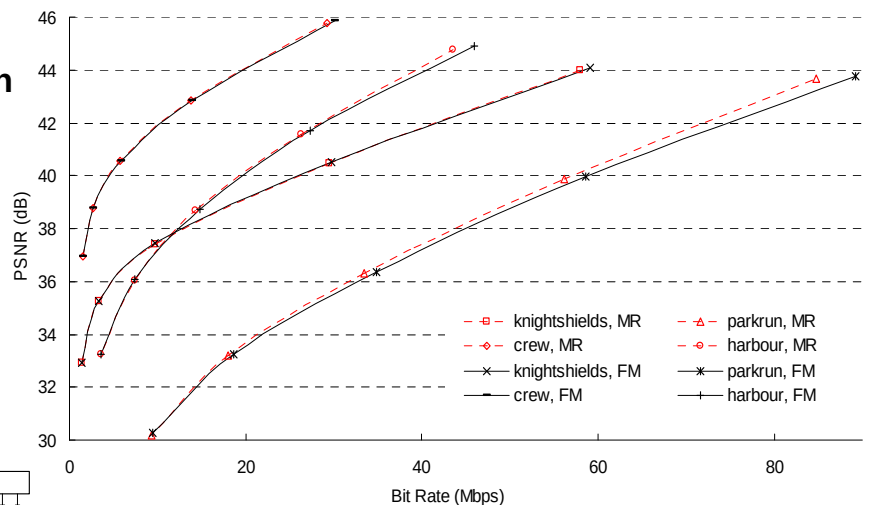
#### ●HDTV 720p

### Hardware Architecture of IME

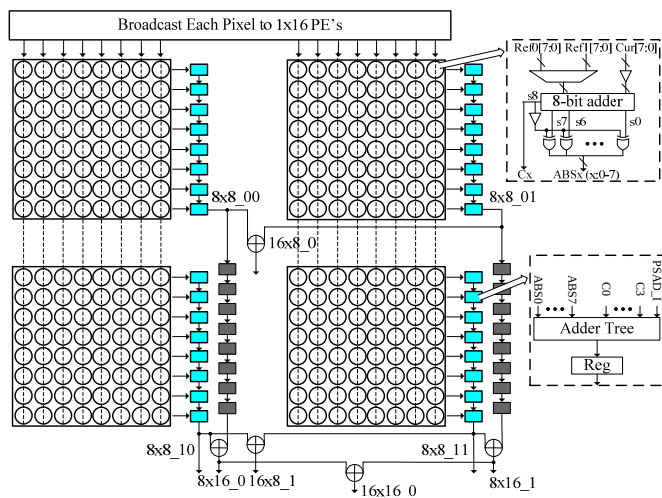
#### ●Mode Reduction impact

#### ●High Speed Impact

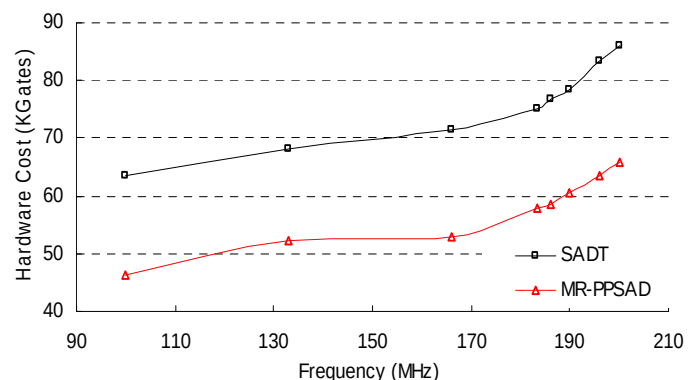
#### ●Adder Tree Improvement



## Existing Structures



○:Processing Element    ■:Row Adder Tree    ■:Shift Register for 8x8



Under frequencies ranging from 100 to 200MHz, MR-PPSAD structure also outperforms SAD Tree when multiple sets of PE array is considered

## Optimized Structure & Hardware Cost Comparison



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