H.264 Real-Time Encoder Research

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1. Fine Granularity and Low Memory Cost VBSME Architecture

Chip Layout (1717*um*✕1713*u*m)

PE Number	256
Search Range	48✕32
Process Technology	TSMC18
Max Frequency	261MHz
Gate Count (SRAM excluded)	151.8K
SRAM Modules	2
PHR	440.2
Granularity	16PEs (8.5K)

2. Low-Pass Filter Based VLSI Oriented VBSME Algorithm

Key Algorithms:

.“Haar” low-pass filter based subsampling

. Simplified Motion Vector Prediction eliminate data dependency in MB

. “Adaptive Sub-search Window” reduces search positions

Simulation Conditions

QP: 28, 30, 32, 34, 36, 38, 40; no B slice; CAVLC; 5 references;
R-D optimization; Hadamard Transform

Simulation Results

Test Sequence	Foreman (QCIF)	coastguard (QCIF)	carphone (QCIF)	news (QCIF)	stefan (CIF)	tempete (CIF)
BDBR	+0.9%	+0.3%	+0.8%	+0.5%	+1.8%	+0.4%
BDPSNR	-0.020dB	-0.011dB	-0.027dB	-0.025dB	-0.044dB	-0.022dB

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