Dual Context Modeling in the EBCOT Unit of JPEG2000 Decoder for Digital Cinema

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Background

2k Master File
2048 x 1080
24/48 fps
X',Y,Z'
12 bit

4k Master File
4096 x 2160
24 fps
X',Y,Z'
12 bit

2k files

4k files

2k Projector

4k Projector

EBCOT Tier 1

Compressed bit-stream → Arithmetic Decoder

Context

Arithmetic Decoder → Decision → Bit-Plane Decoder

Bit-Plane Decoder → Wavelet coefficients
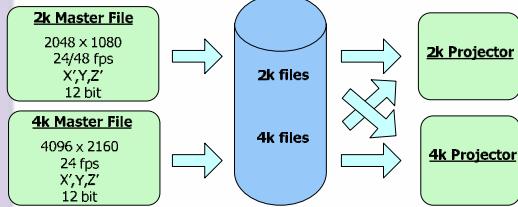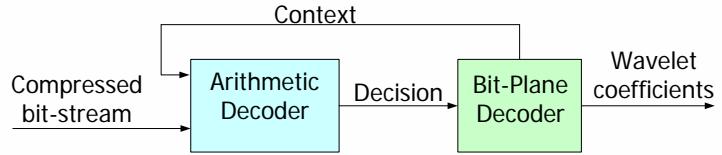
Processing Speed — Throughput of BPD is not sufficient

Hardware size — Increase throughput   Hardware cost increase

Proposal 1

Current pixel
Dependent to next pixel
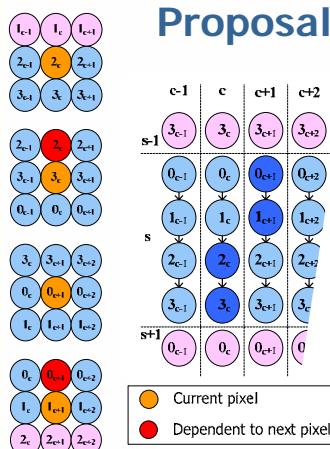
Restrict dependence on decision bits
- Reduction of clock cycles

4 column's status data are stored in register
- Negligible increase in hardware size

Software simulator

Verify functionality

Estimate performance

Number of clock cycles

Test pattern	Clocks/code-block		Decreased percentage
	Conv. 1	Prop. 1	
Test pattern 1	2820	2572	8.79 %
Test pattern 2	2671	2453	8.14 %
Test pattern 3	3159	2891	8.48 %

Proposal 2

Set 0

Set 1

Predict next column

Reduction of clock cycles

Reduction of Hardware cost

Throughput Estimation

Throughput, MByte/s

Decoders in parallel

Conventional 2
Proposal 2

Hardware Architecture

Control Unit

Sample Skipping

Predict Unit

Combined memory
δ', π', ν, χ

128 x 32 bit

Register 6 x 32 bit

Pass Flag Generation

Context Window

Arithmetic Decoder

Decision
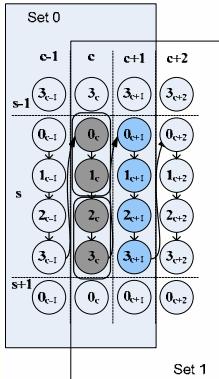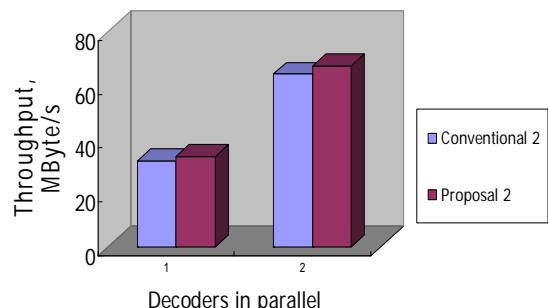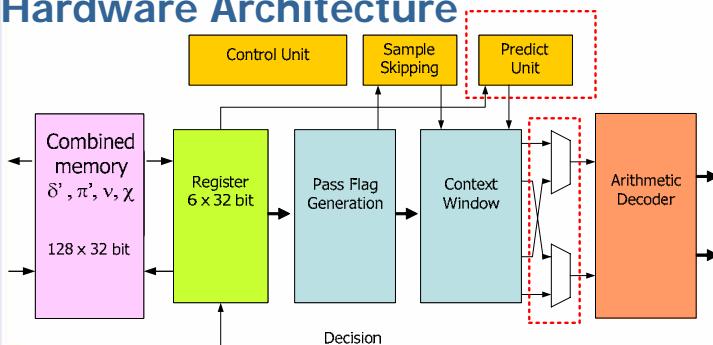
Technology	TSMC0.18	
Synthesis tool	Synopsys Design Compiler	

Sub block	Conventional		Proposed	
	Gates	Delay [ns]	Gates	Delay [ns]
Prediction unit	-	-	412	0.58
Sample skipping	6241	2.41	5970	1.92
Context window	11043	2.63	8135	2.63

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